IN THE SPECIFICATION

Please amend the Title on page 1 as follows:

NONVOLATILE SEMICONDUCTOR MEMORY ~~DEVICE~~ HAVING SELECTIVELY CONTROLLED MEMORY CIRCUITS

Please replace the paragraph beginning at page 1, line 5, with the following rewritten paragraph:

This application claims benefit of priority under 35 U.S.C. § 119 to Japanese Patent Application No. ~~Hei11~~ Hei 11-349388 (1999), filed on December 8, 1999, the entire contents of which are incorporated by reference therein.

Please replace the paragraph beginning at page 1, line 11, with the following rewritten paragraph:

The present invention relates generally to an ~~electrically rewritable nonvolatile semiconductor memory device~~ Electrically Erasable Programmable Read Only Memory (EEPROM). More specifically, the invention relates to an EEPROM wherein a series of rewriting operations including verify operations are automatically sequentially controlled by a control circuit included in the EEPROM.

Please replace the paragraph beginning at page 1, line 26, with the following rewritten paragraph:

Such a waiting time in the busy state of the EEPROM flash memory adversely affects the high-speed performance of a memory system. Therefore, in order to realize a high-speed performance in a flash memory system using a plurality of memory chips, it is effective to commonly use a data bus for time-sharing inputting commands and data to carry out internal

operations in the plurality of memory chips in parallel. The inventors have proposed such a technique (Japanese ~~Patent Application~~ Publication (Kokai) Nos. 6-95125 and 6-95126, US Patent No. 5,603,001, etc.).

Please replace the paragraph beginning at page 2, line 8, with the following rewritten paragraph:

As circumstances on the side of a Central Processing Unit CPU for controlling a memory system, there are also circumstances wherein even if the storage capacity of a required memory system increases, the size of a handled file other than image files often does not remarkably increase, and many small-size files are rather preferably handled. The page mapping size of the CPU of personal computers is also maintained to be, e.g., 4 kilobytes, as a common value regardless of the generation of the CPU.

Please replace the paragraph beginning at page 3, line 14, with the following rewritten paragraph:

According to the present invention, a plurality of memory circuits (EEPROM circuits) in a single chip can be operated in time sharing or in parallel as if ~~a plurality chip~~ plurality chips are operated. Therefore, unlike a case where the storage capacity of a single chip is simply increased by a single control circuit, even if a certain circuit is in a busy state, it is possible to access other memory circuits, so that it is possible to obtain a high-speed performance memory system without waiting time at sight from the outside.

Please replace the paragraph beginning at page 3, line 14, with the following rewritten paragraph:

FIG. 2 is a block diagram showing the construction of each of the EEPROMs in the preferred embodiment;

Please replace the paragraph beginning at page 3, line 34, with the following rewritten paragraph:

FIG. 2 is a block diagram showing the construction of each of the EEPROMs in the preferred embodiment;

Please replace the paragraph beginning at page 4, line 28, with the following rewritten paragraph:

FIG. 2 shows the construction of each of the EEPROM circuits 2. A memory cell array 21 has electrically rewritable nonvolatile memory cells which have a stacked gate structure and which are arranged and connected so as to form a NAND type. The word and bit lines of the memory cell array 21 are selected by a row decoder 22 and a column decoder 25, respectively. An address signal is incorporated into an address register 27, via an input/output I/O buffer, 26 to be decoded by the row decoder 22 and the column decoder 25 to select a memory cell. The bit lines of the memory cell array 21 are connected to a sense amplifier 23 which is connected to the I/O buffer 26 via a data register 24.

Please replace the paragraph beginning at page 5, line 2, with the following rewritten paragraph:

In order to generate various high voltages for use in data writing and erasing, a booster power supply circuit 30 is provided. A control circuit 29 is designed to sequentially control data writing and erasing including verify operations, and simultaneously control the booster power supply circuit 30 in accordance with an operation mode. A command CMD for writing or erasing is incorporated into a command register 28 via the I/O buffer 26. The command incorporated into the command register 28 is decoded by the control circuit 29 to control writing or erasing in accordance with the command. Various enable signals including

enable signals /CE, which are ~~outputted from~~ input to the chip enable terminals CE and which are indicative of the activity and inactivity of the whole circuit, enter the I/O buffer 26. These ~~control~~ signals are also fed to the control circuit 29. The control circuit 29 outputs a busy signal to the terminal R/B via a Ready/Busy buffer 31 when the enable signal ~~is~~ /CE = H.

Please replace the paragraph beginning at page 5, line 22, with the following rewritten paragraph:

As described above, according to this preferred embodiment, a plurality of EEPROM circuits having an autonomous control function are provided in a single chip, so that it is possible to operate the EEPROM circuits in parallel to carry out a high-speed operation of a large-capacity memory. Each of the EEPROM circuits is provided with a chip enable terminal and a Ready/Busy terminal corresponding thereto, so that it is possible to control each of the EEPROM circuits from the outside as an independent memory chip. Therefore, unlike a case where the storage capacity of a single chip is simply increased, it is possible to realize a high-speed performance, and it is possible to flexibly cope with a request ~~to input/output data every small capacity unit~~ for inputting/outputting by small unit of storage capacitor.

Please replace the paragraph beginning at page 6, line 13, with the following rewritten paragraph:

With such a construction, it is possible to decrease the number of ~~enable~~ signal lines which extend from a chip set for controlling a memory system comprising a plurality of memory chips.

Please replace the paragraph beginning at page 6, line 31, with the following rewritten paragraph:

Specifically, when a memory system is constructed as shown in FIG. 4, the operation of a chip set for controlling the memory, system in response to host-side requests is as follows. That is, it is assumed that the host's requests includes only the assignment of the chip enable terminals CE1 through CE4 and an address assignment. In this case, the chip set refers to ~~the storage capacity resistor~~ a storage capacity register of the EEPROM circuits 2 of the memory chips 1a1 and 1a2 to determine "0" or "1" of the master chip enable terminal MCE. Then, the chip set issues a master enable signal together with the assignment of the chip enable terminals CE1 through CE4 and address assignment, which are host's requests. Thus, any one of the memory chips la1 and la2 is selected.

Please replace the paragraph beginning at page 7, line 10, with the following rewritten paragraph:

FIG. 5 shows another preferred embodiment of a memory chip 1b according to the present invention. The difference between this preferred embodiment and the preferred embodiment shown in FIG. 1 is that only one chip enable terminal CE and only one Ready/Busy terminal R/B are provided ~~outside~~. The chip enable terminals CE1 through CE4 and Ready/Busy terminals R/B1 through R/B4 of EEPROM circuits 2 are internally selected by a memory function register 4.

Please replace the paragraph beginning at page 7, line 18, with the following rewritten paragraph:

It is assumed that a memory function ~~selecting circuit 3~~ register 4 is controlled by inputting a command. For example, when the chip enable CE is activated to input a

command to indicate that the chip enable terminal CE1, i.e., the EEPROM circuit 2-1, is selected, the memory function register 4 causes the chip enable CE to be ~~enable~~ enabled with respect to the EEPROM circuit 2-1. At this time, the Ready/Busy terminal R/B outputs the Ready/Busy state of the EEPROM circuit 2-1. When the chip enable CE is deactivated, the chip enable with respect to the whole memory chip 1b is negated.

Please replace the paragraph beginning at page 7, line 28, with the following rewritten paragraph:

If access sorting is thus carried out with respect to the plurality of EEPROM circuits in the memory chip, it is possible to control a large-capacity memory system by the same number of signal terminals as that in the case of a single EEPROM circuit. Therefore, the same CPU can be connected to ~~any one of memory chips, the generation~~ any one of a number of memory chips, the generation of which are different, by only the change of a software.

Please replace the paragraph beginning at page 7, line 35, with the following rewritten paragraph:

When the chip enable signal CE is deactivated, ~~a little control continues to enter~~ the control is not often continued for each of the EEPROM circuits. Therefore, if the selection to each of the EEPROM circuits is released in connection therewith, the release of the selection can be easily controlled, and the subsequent control can be easily carried out.

Please replace the paragraph beginning at page 8, line 12, with the following rewritten paragraph:

FIG. 6 shows a preferred embodiment of a memory chip 1c according to the present invention as a modification of the preferred embodiment shown in FIG. 5. The ~~different~~

difference between the memory chip 1c in this preferred embodiment and the memory chip shown in FIG. 5 is that the memory chip 1c does not ~~has~~ have the chip enable terminal and Ready/Busy terminal outside and has a Ready/Busy register 5 for realizing their functions by ~~a~~ software. In this preferred embodiment, various commands CMD include a chip enable control command and a Ready/Busy reference command.

Please replace the paragraph beginning at page 8, line 27, with the following rewritten paragraph:

According to such a preferred embodiment, it is not required to scan the signal terminals in order to monitor the Ready/Busy signal of each of the EEPROM circuits. Therefore, it is also not required to estimate a delay in switching transition time, such as a case where the same signal line is switched to output the Ready/Busy signal of each of the EEPROM circuits. Moreover, if a command control can acquire the Ready/Busy states of the respective EEPROM circuits at a time, it is possible to carry out ~~a~~ one high-speed operation control.

Please replace the paragraph beginning at page 8, line 36, with the following rewritten paragraph:

If the memory chip is designed to operate in a conventional memory chip specification interchangeable mode (i.e., a specification wherein it is not ~~felt~~ recognized that a plurality of EEPROM circuit functions are provided inside) in an initialization state in which no command control is carried out, the system can be applied directly to conventional apparatuses. Moreover, if the state of the memory chip can be returned to the initial state by issuing a reset command, it is possible ~~two return~~ to initialize the memory chip when the

abnormality on the side of the software is processed, so that it is possible to obtain a memory system having a ~~high recovery~~ high resiliency.

Please replace the paragraph beginning at page 9, line 25, with the following rewritten paragraph:

According to this preferred embodiment, while data are written by, e.g., an EEPROM circuit 2-1, data can be inputted from the outside to other EEPROM circuits 2-2 through 2-4, so that ~~continuously~~ continuous data writing operations can be carried out from the outside ~~in~~ with no waiting time.

Please replace the paragraph beginning at page 10, line 8, with the following rewritten paragraph:

When the writing starting command "15" is inputted, data having been held by the latch provided in the I/O buffer of each of the EEPROM ~~circuit~~ circuits 2 are simultaneously transferred to the internal data register 24. Thus, a writing operation is started in a page which has been selected by addresses in the respective EEPROM circuits 2 in parallel. When data writing is started, each of the EEPROM circuits 2 alternately carries out writing and verify until writing end conditions are automatically satisfied. When the batch data transfer to the internal data register is completed, the state becomes a ready state to the outside.

Please replace the paragraph beginning at page 10, line 18, with the following rewritten paragraph:

Preferably, in this preferred embodiment, the Pass/Fail result of the writing operation of each of the EEPROM circuits 2 is not only outputted, but the Pass/Fail result of the whole memory chip ld is also outputted. Thus, each of the EEPROM circuits 2 can ~~process the~~

process in case of Fail, and if the whole Pass/Fail can be recognized, it is possible to determine whether the processing is continued or stopped, without referring to the written result of each of the EEPROM circuits 2.

Please replace the paragraph beginning at page 10, line 26, with the following rewritten paragraph:

In this preferred embodiment, the accumulated Pass/Fail results of the writing operations, which have been repeatedly carried out with respect to each of the EEPROM circuits 2, are preferably held to output information about the ~~presence of Fail~~ existence of failure during accumulation. Thus, ~~the whole~~ the overall Pass/Fail can be determined after all of a series of writing operations are completed. In particular, when a writing cache like operation is carried out, a series of operations can be continuously carried out, so that it is possible to carry out a high-speed performance processing.

Please replace the paragraph beginning at page 10, line 35, with the following rewritten paragraph:

It is considered that the accumulation of the Pass/Fail results is carried out ~~every~~ for each EEPROM or as a whole memory chip. In the former, it is possible to carry out a processing in the case of Fail ~~every~~ for each EEPROM circuit~~, and in~~. In the latter, it is not required to refer to each of the EEPROM circuits in the case of Pass.

Please replace the paragraph beginning at page 11, line 4, with the following rewritten paragraph:

In this preferred embodiment, it is preferably possible to select one of a mode, in which the next data are inputted to the data buffer after referring to the Pass/Fail result of data

writing, and a mode, in which data are continuously inputted to the data buffer without referring to the Pass/Fail result. In this case, the meaning of how to output a Busy signal is different in the respective modes. That is, in the former mode, it is assumed that the Busy state is completed when the state of the written result can be referred. In this case, since the data writing is actually completed, the next data can be ~~inputted~~ input In the latter, it is assumed that the Busy state is completed when the next data writing can be carried out.

Please replace the paragraph beginning at page 11, line 16, with the following rewritten paragraph:

By enabling one to carry out such a mode selection, a high-speed processing and a stable processing can be selected. If this mode selection can be carried out by inputting a command, the control software can be simplified.

Please replace the Abstract beginning at page 15, line 1, with the following rewritten paragraph: